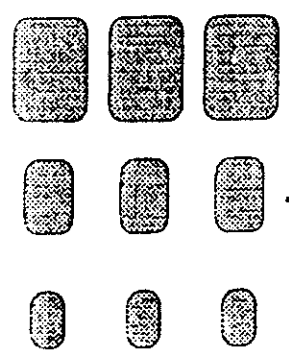


HP
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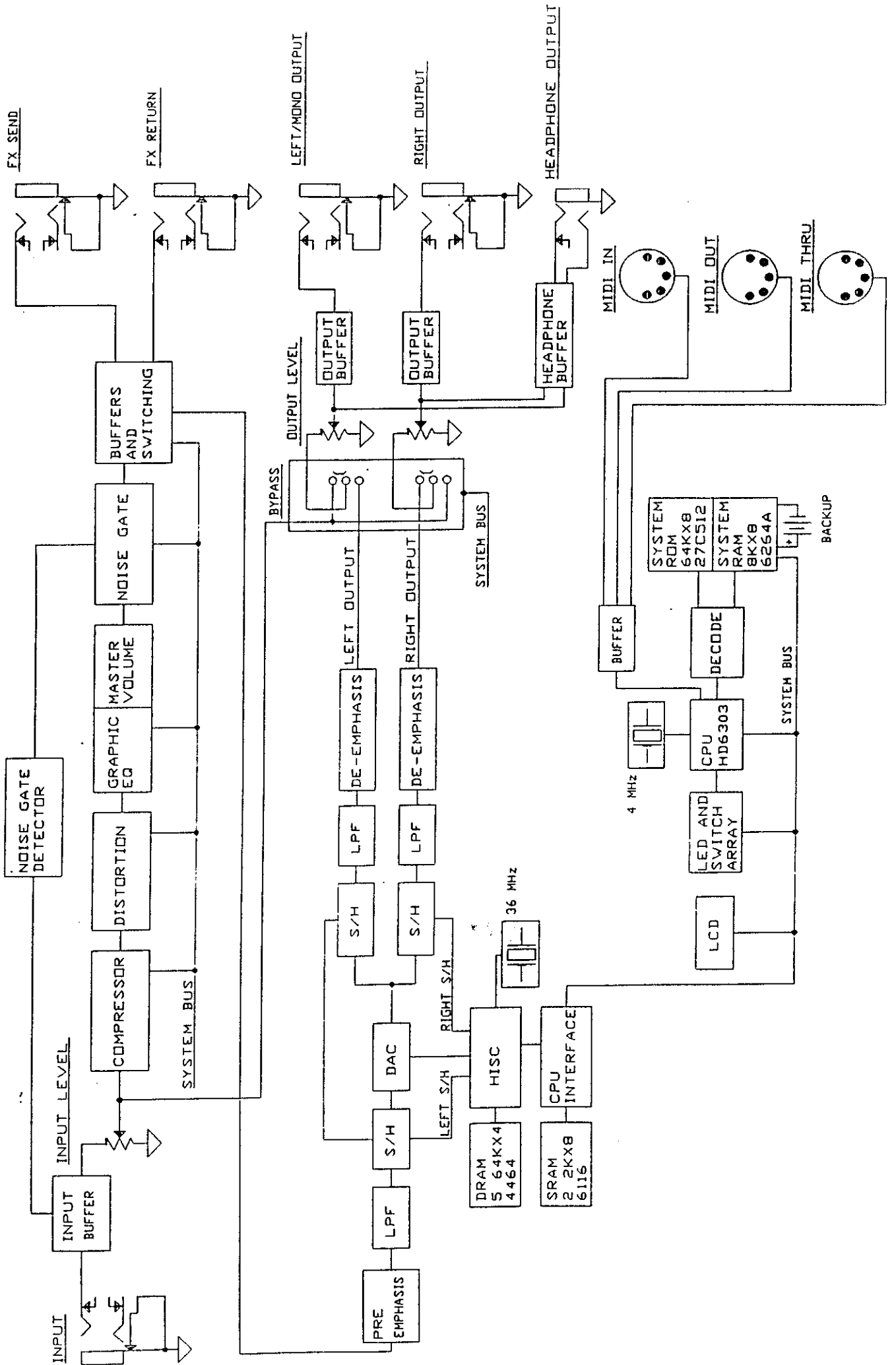


HP-1

Service Manual

- BLOCK DIAGRAM
- SETUP PROCEDURES
- SCHEMATIC DIAGRAMS
- PARTS LISTS
- PC BOARDS
- HISC PINOUT
- HISC PIN DESCRIPTIONS

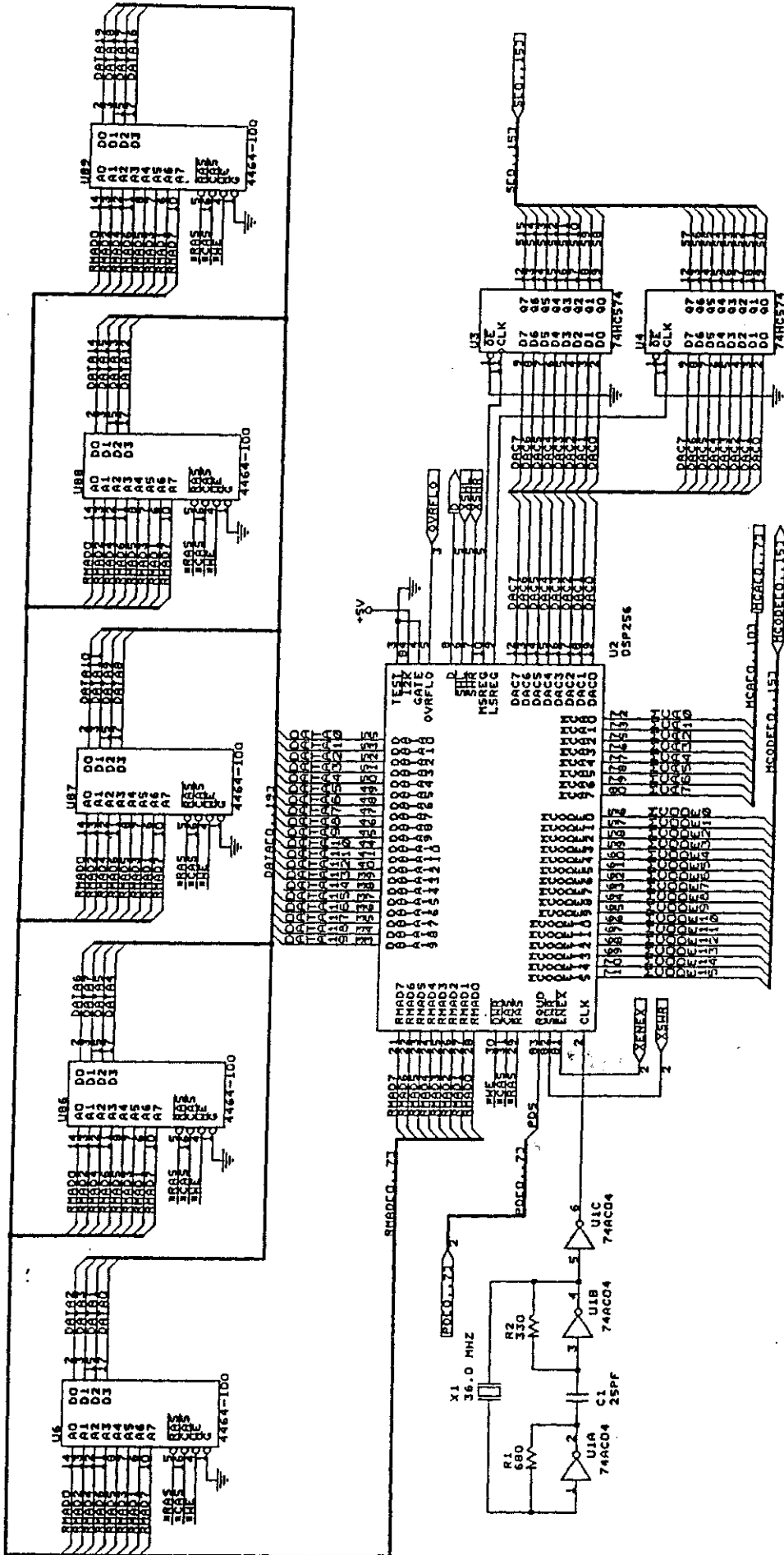
RP4 BLOCK DIAGRAM



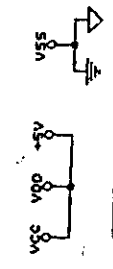
RP-1 Setup and Test Procedures

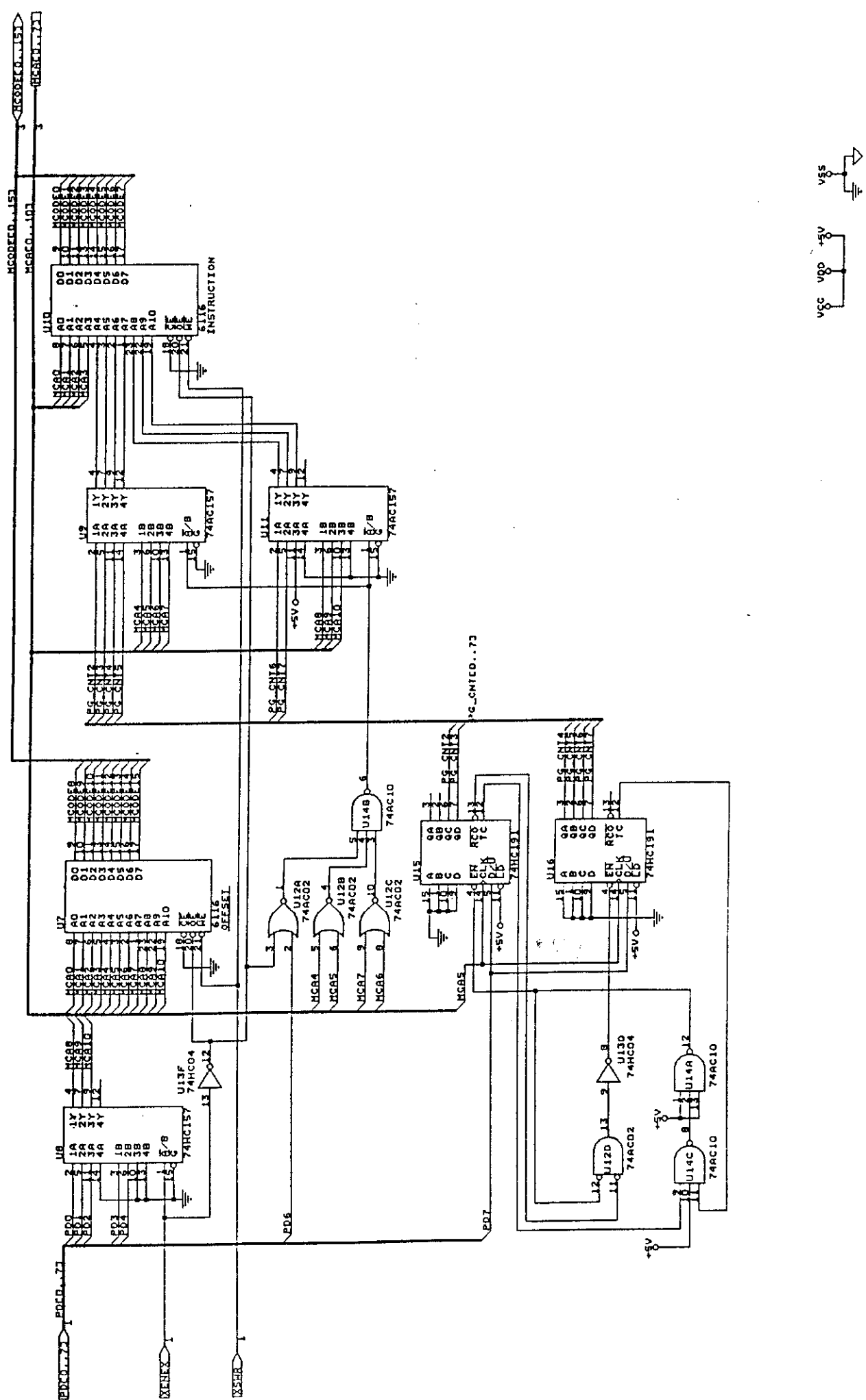
To access the RP-1 setup and test menus, enter the UTILITY mode and scroll left or right until the software version number is displayed. Press the parameter down button twice to enter the test menu. Scroll right to access the compressor gain trim, distortion gain trim, and A/D calibration programs. The procedures for these setup routines are detailed below. Further scrolling will show the EQ test, speaker simulator test, compression test, distortion test, noise gate test, HISC test, RAM test, and display tests. When done, return to the main utility menu.

1. Compressor gain trim: With a 1 Vp-p, 1 KHz sine wave measured at test point one (TP1) on the main PCB, adjust P6 (50K trimpot) until the signal measured at TP4 is the same amplitude as the signal at TP1.
2. Distortion gain trim: Adjust P7 (50k trimpot) until the voltage measured at pin 7 of U97 is between -3mV DC and +3mV DC.
3. A/D Calibration
 - a) Gain: With a 14 Vp-p, 1KHz sine wave measured at TP2, adjust P2 (10K trimpot) until the signal measured at TP3 is 14 Vp-p.
 - b) Bias: Reduce the signal level 50 dB to 44.3 mVp-p and adjust P3 (50K trimpot) until the signal seen at TP3 is just barely all positive going or all negative going.

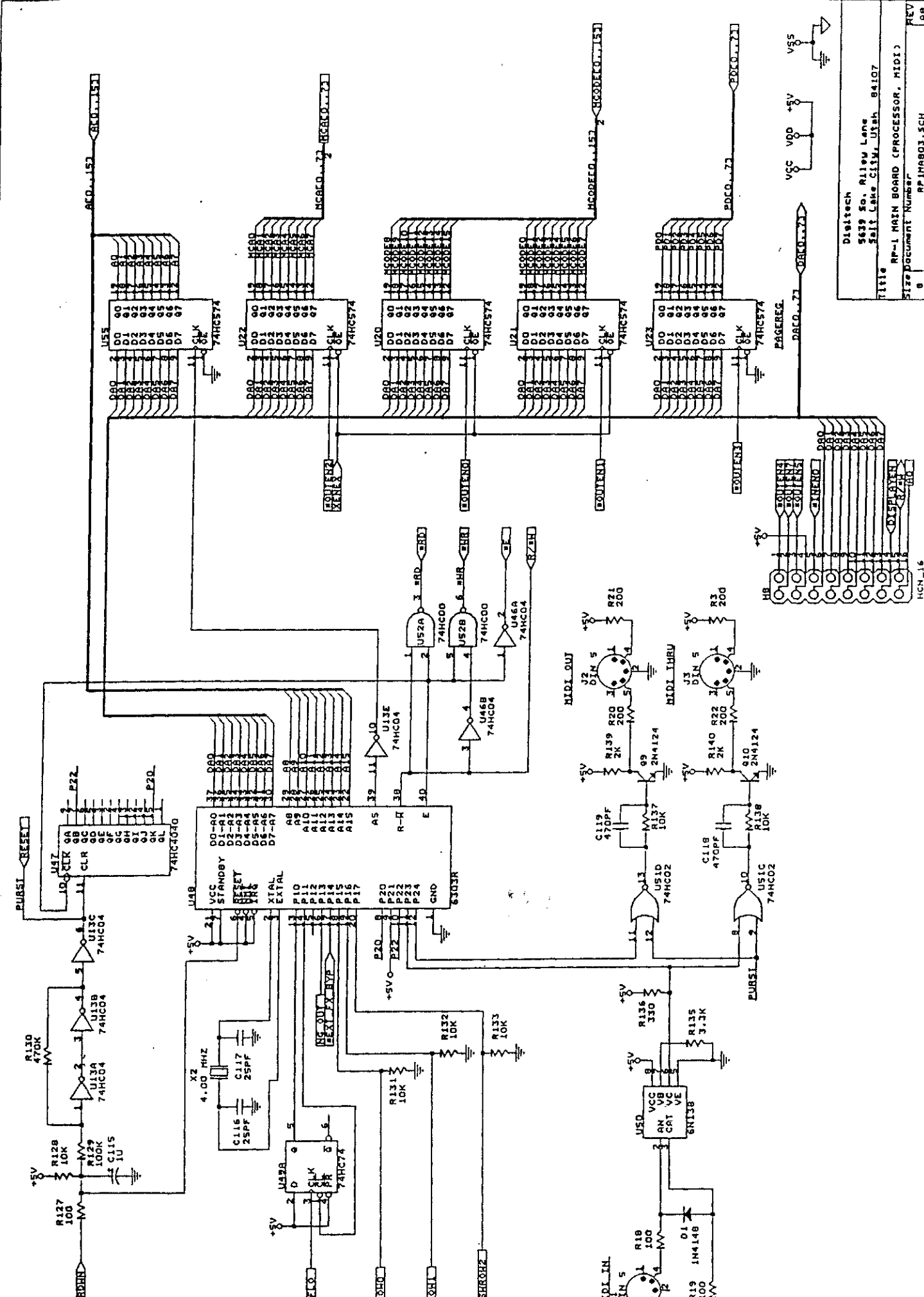


- IRP1M8B01.SCH
- IRP1M8B02.SCH
- IRP1M8B03.SCH
- IRP1M8B04.SCH
- IRP1M8B05.SCH
- IRP1M8B06.SCH
- IRP1M8B07.SCH
- IRP1M8B08.SCH
- IRP1M8B09.SCH
- IRP1M8B70.SCH

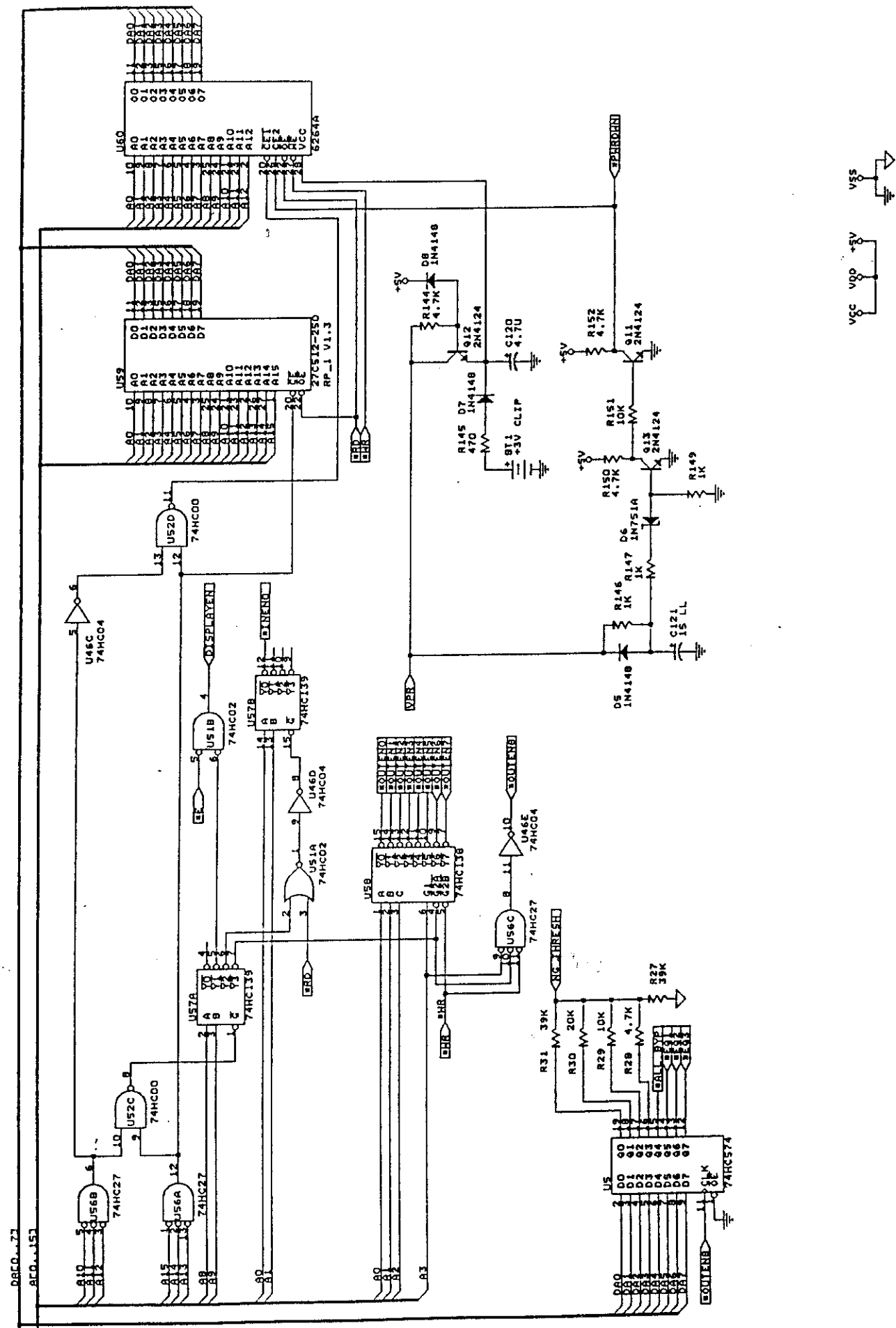




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 Salt Lake City, Utah 84107
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 Size Document Number B
 Rev AP1MAB02.SCH 1A
 Date May 19, 1992 15:55 2.07 10

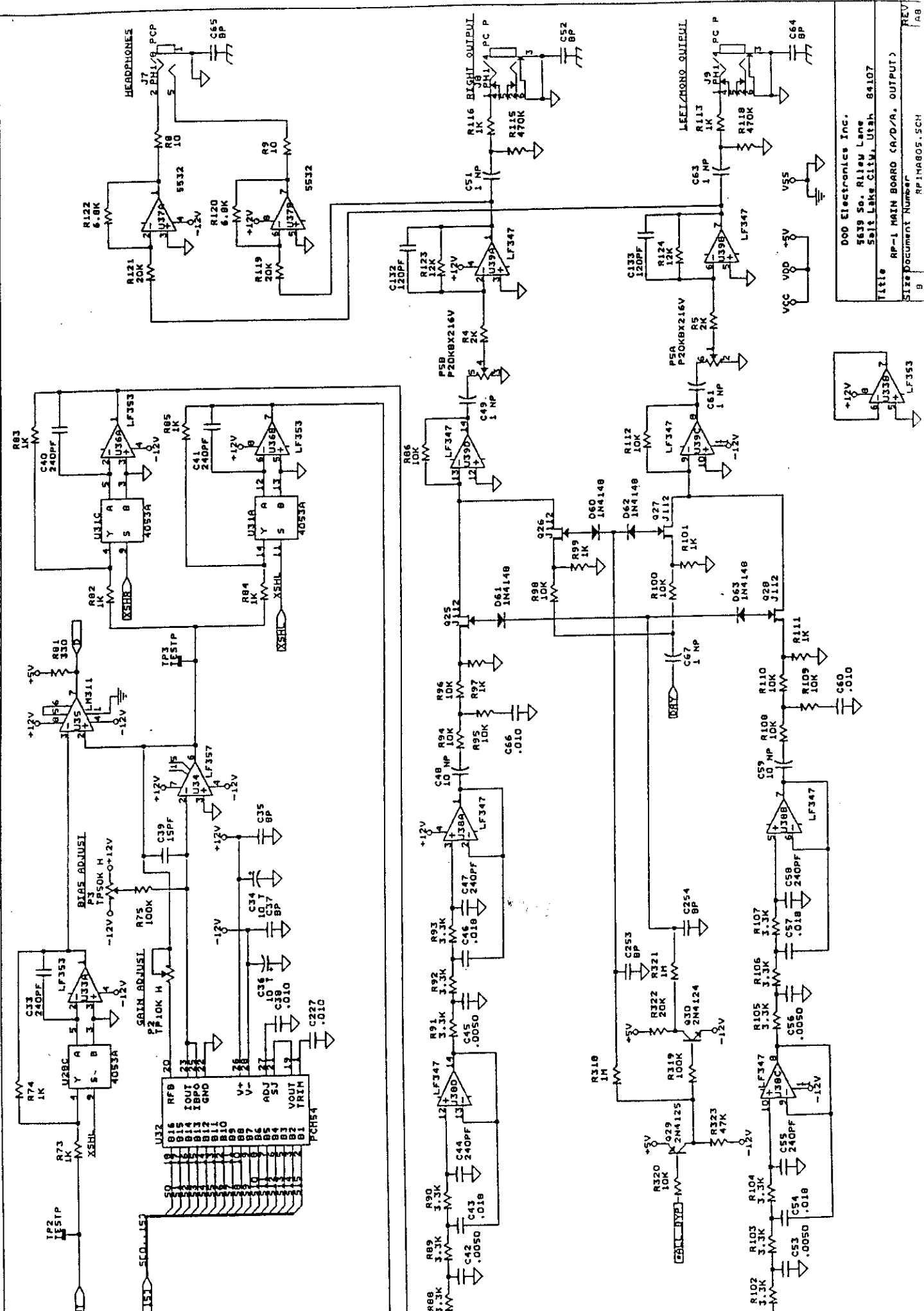


Dislitech
 5639 So. 811th Lane
 811 Lane Cliv, Utah 84107
 Title RP-1 MAIN BOARD (PROCESSOR, MIDI)
 Size Document Number 8
 Rev 18 12/27/87 HCN_16



D1eitech
 8639 So. Riley Lane
 Salt Lake City, Utah 84107
 Title RP-1 MAIN BOARD (EPROM, SRAM, DECODE)
 Size Document Number RP1M804.SCH
 Date 10/28/83 13:52:58 4 of 8



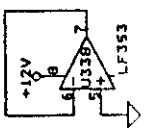


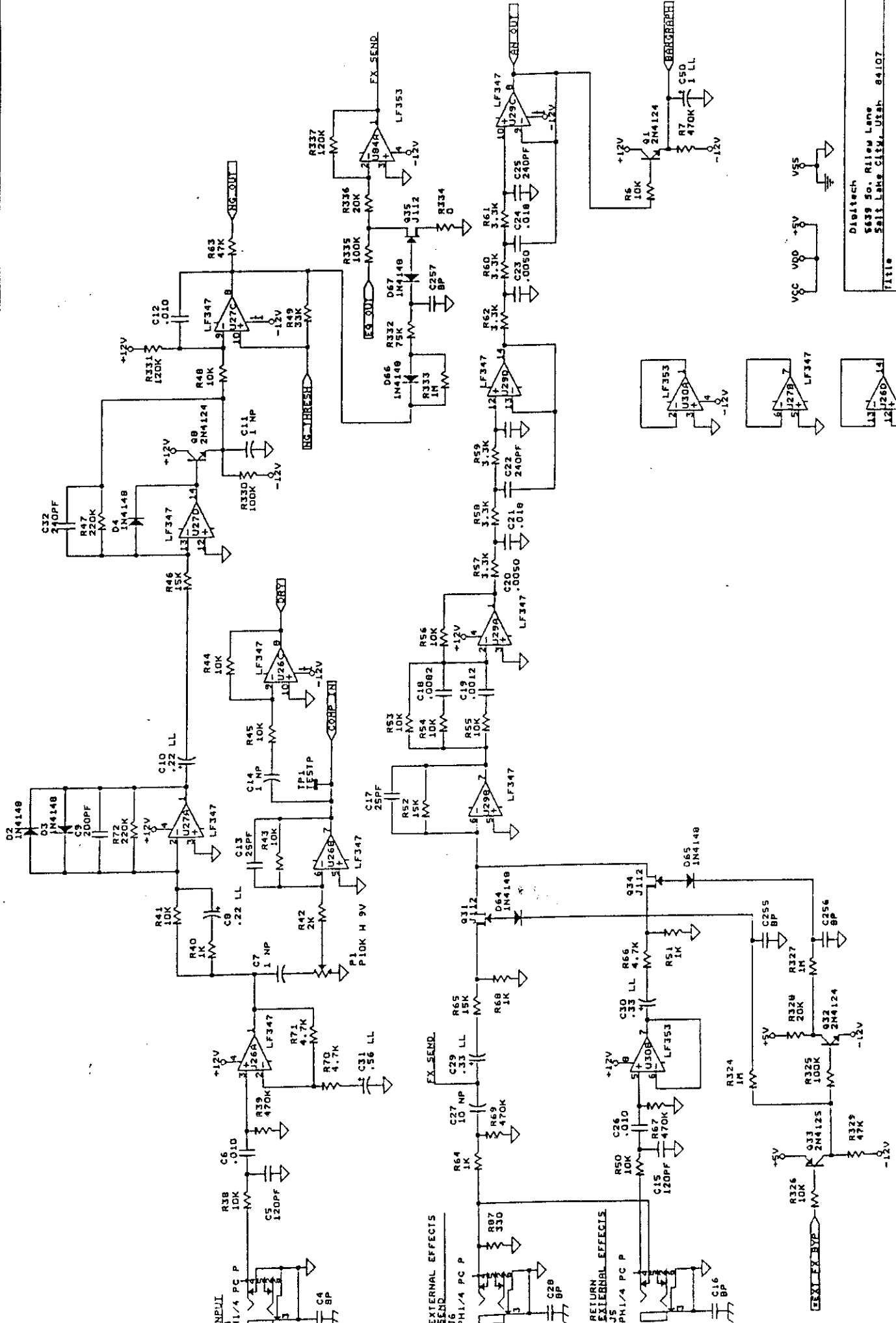
DOD Electronics Inc.
 3639 So. Rilliew Lane
 Salt Lake City, Utah 84107

Title: RP-1 MAIN BOARD (A/D/A. OUTPUT)

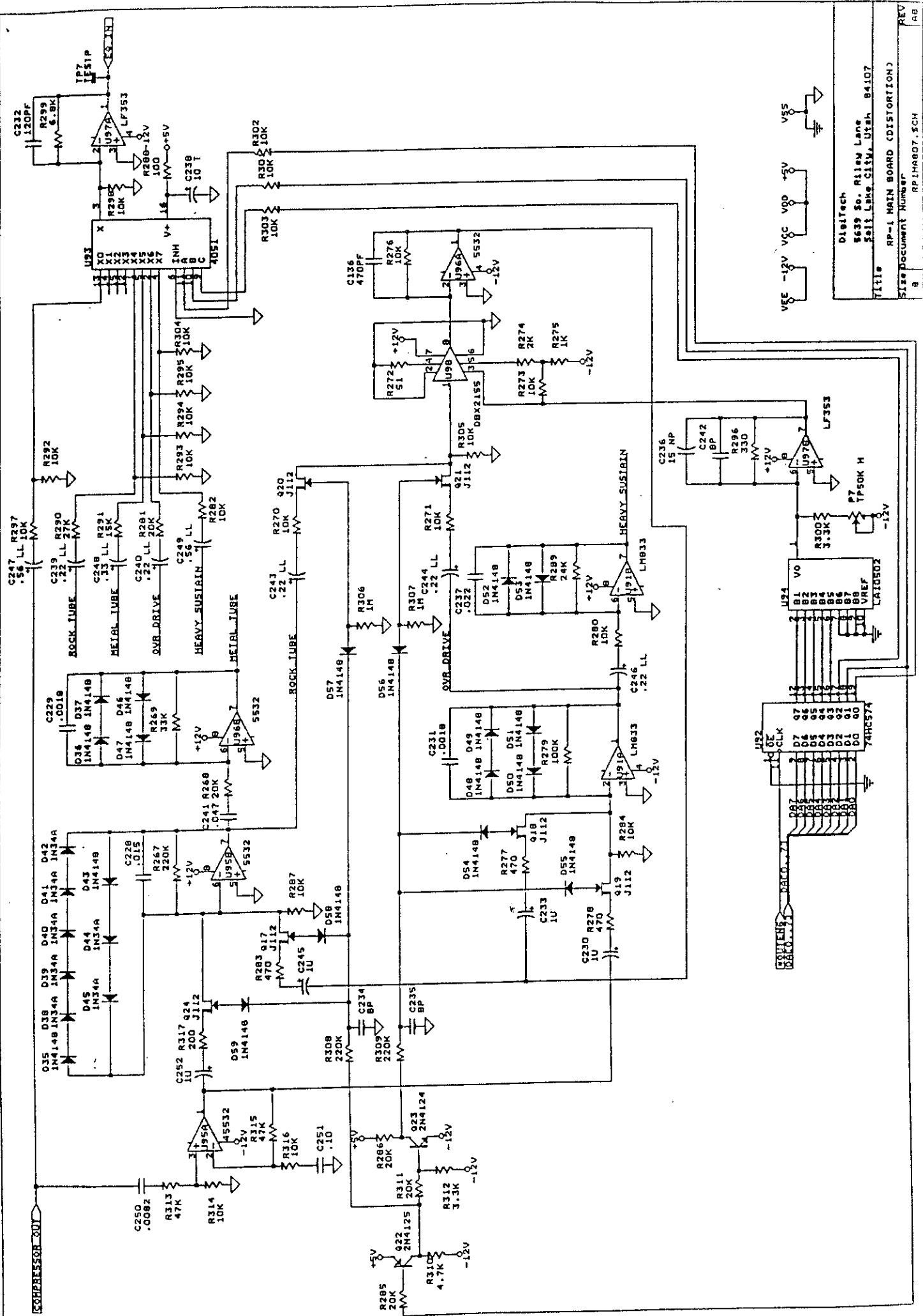
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REV: B

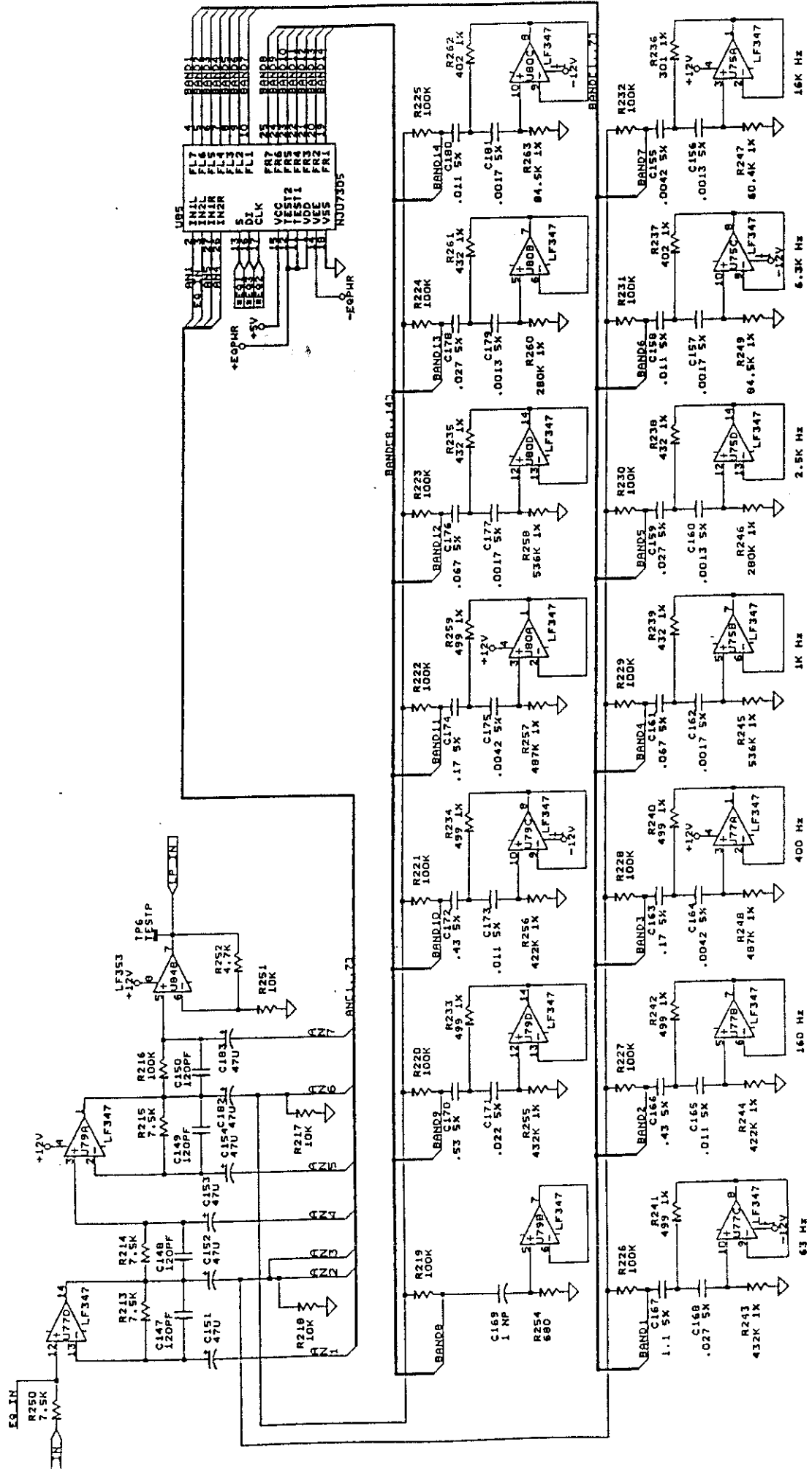




Disltech
 5839 So. Riley Lane
 Salt Lake City, Utah 84107
 Title
 AP-1 MAIN BOARD (INPUT, GATE, FX LOOP)
 Size Document Number
 8
 RPIH806.SCH
 REV
 A8

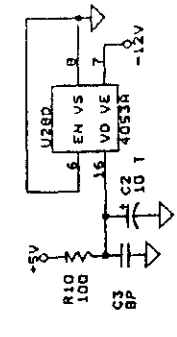
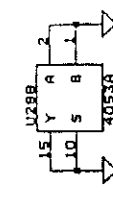
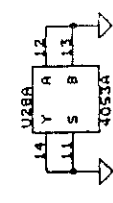
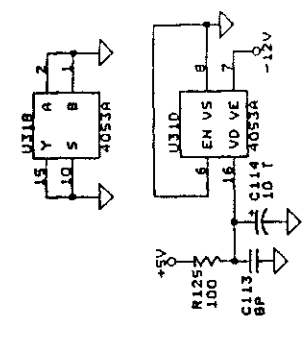
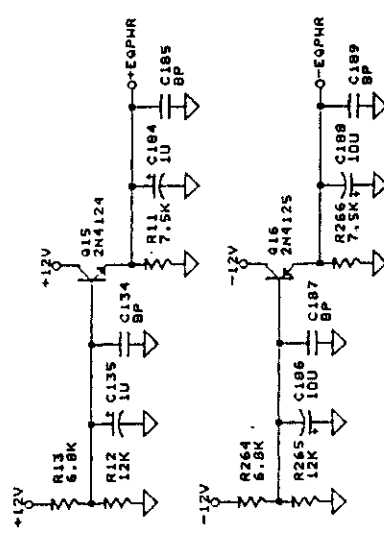
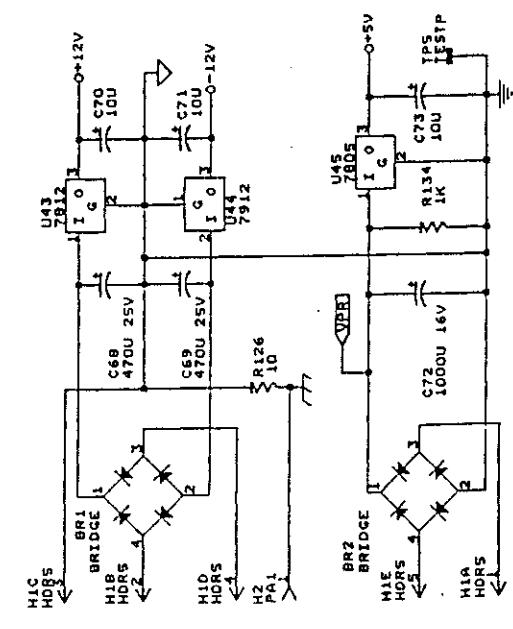
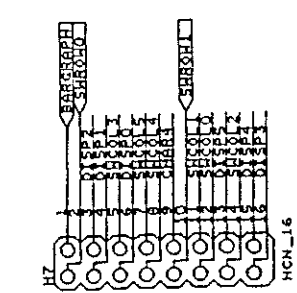
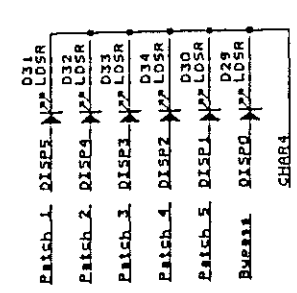
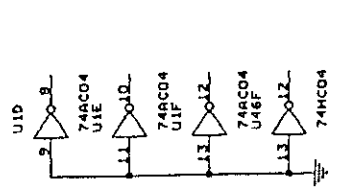
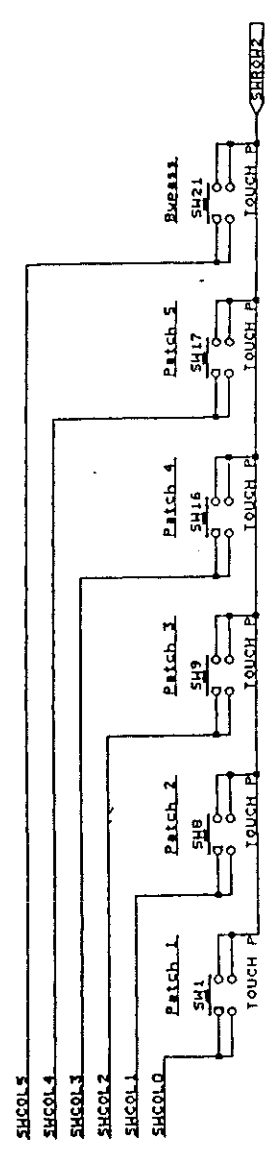


VEE -12V VCC +5V VSS
 Digitech
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 Salt Lake City, Utah 84107
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 Size: Document Number: RPHAB07.SCH
 8 REV: 1A

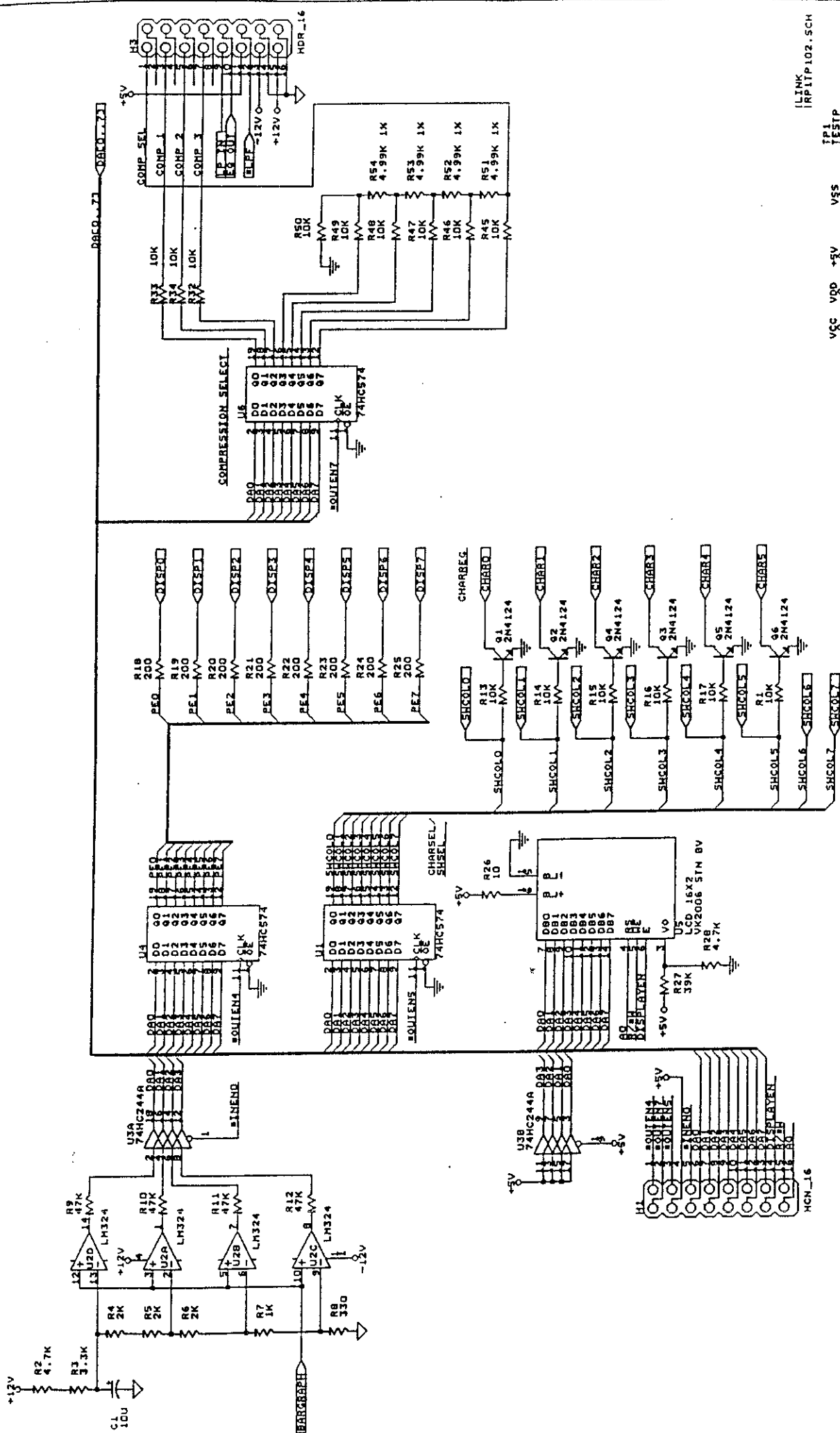


DOD Electronics, Inc.
 5639 So. Ritten Lane
 Salt Lake City, Utah 84107
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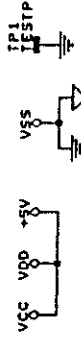




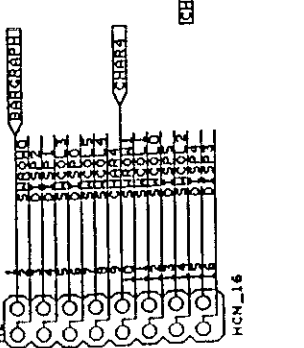
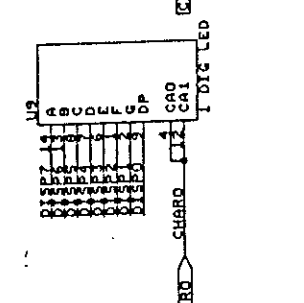
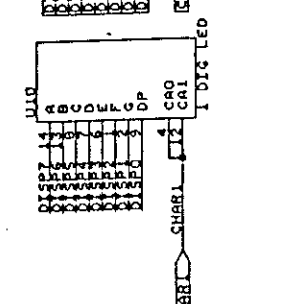
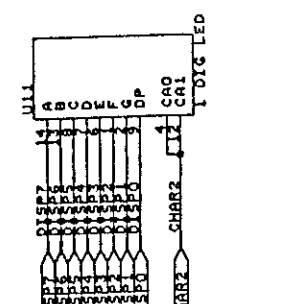
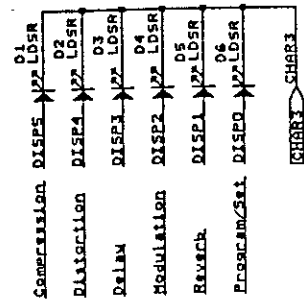
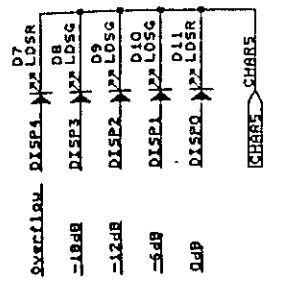
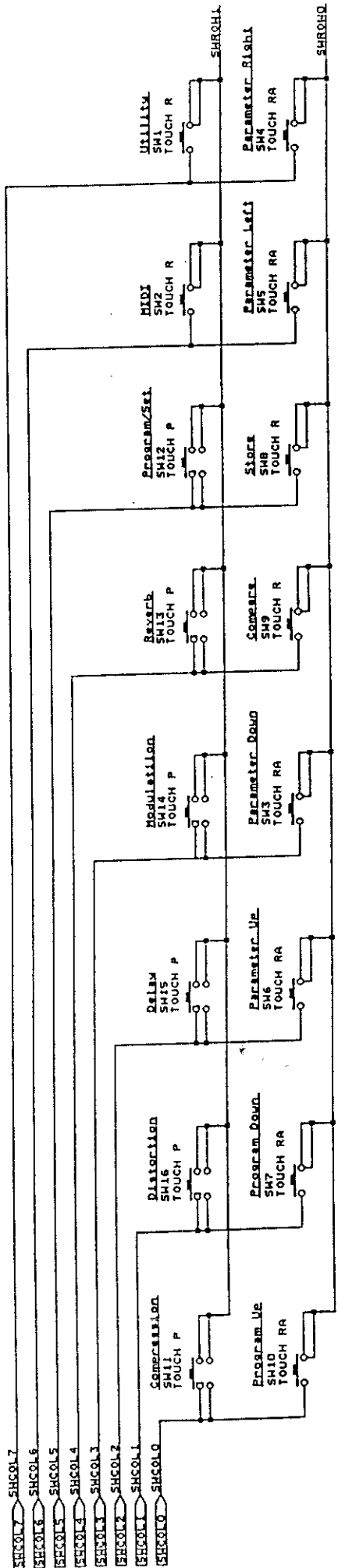
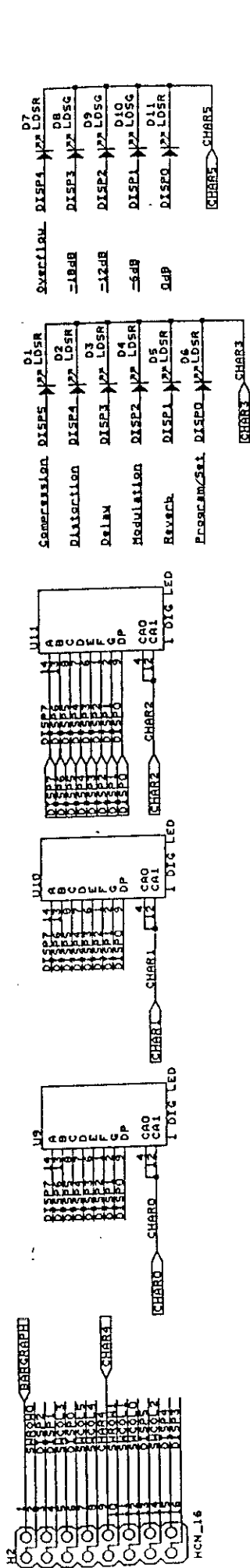
- NOT USED
- C137-156
 - C192-201
 - C203-210
 - D12-28
 - H4-5
 - Q1-7
 - Q14-17, 23-26
 - R16-80
 - R114, 117
 - R141-143, 171-173
 - R177
 - R184, 212, 253
 - TPS
 - U17-19, 24-25
 - U40, 42, 53-54
- LAST REF.
- BR2
 - BL1
 - C257
 - D67
 - H8
 - P10
 - Q15
 - R337
 - R337
 - S21
 - Y9
 - Y1



LINK
IRPLTP102.SCH

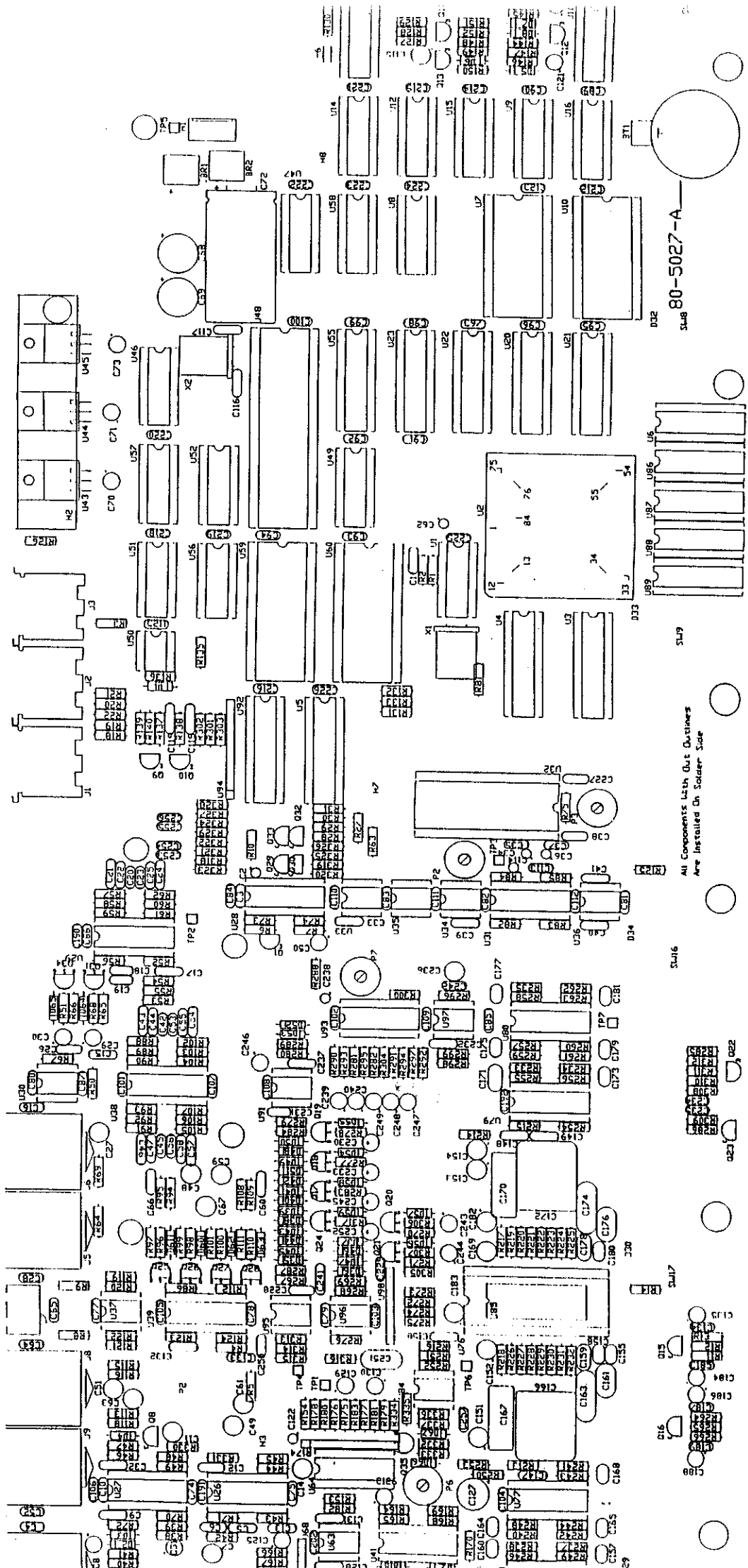


Digitaltech
3639 So. Rileys Lane
Salt Lake City, Utah 84107
Title RP-1 TOP BOARD (LCD, HEADROOM)
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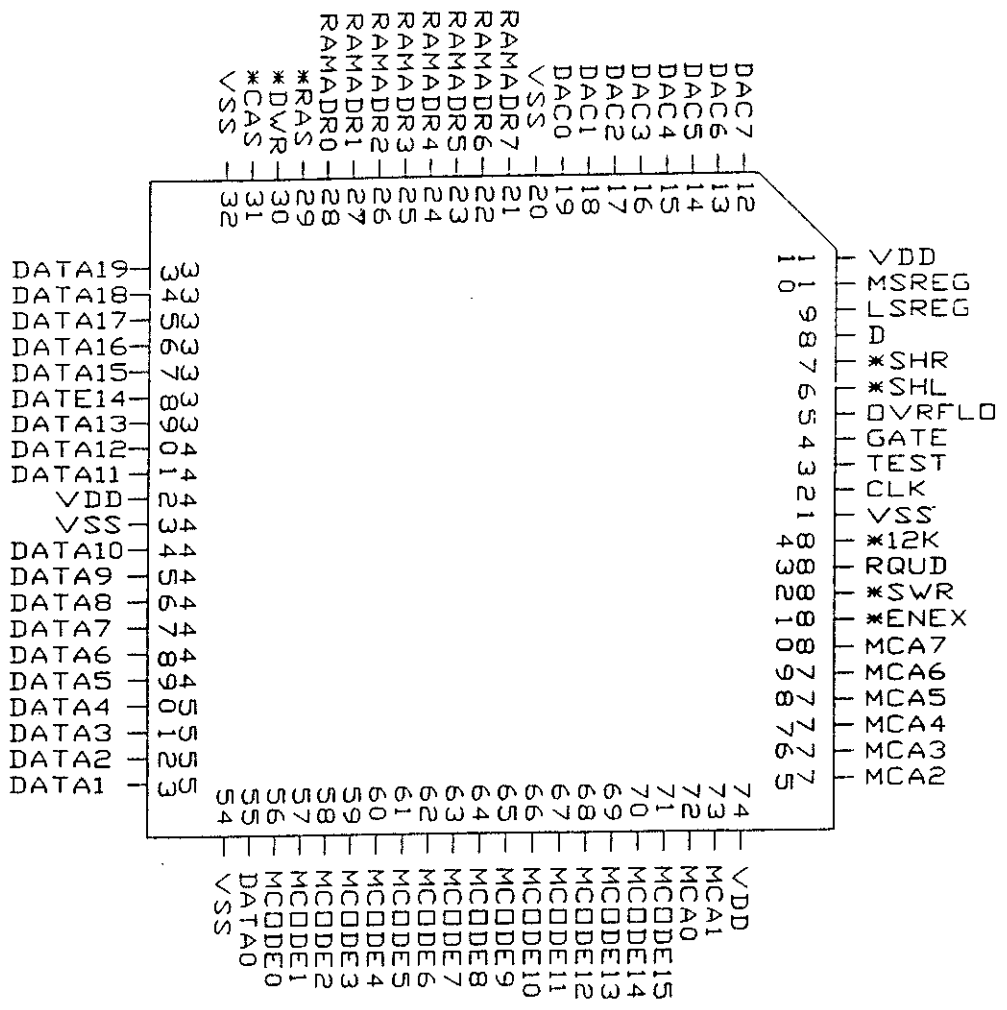
Disteltech
 5639 So. Riley Lane
 Salt Lake City, Utah 84107
 Title
 RP-1 TOP BOARD (SWITCHES, LEDS)
 Size Document Number
 8 RPL10002.SCH
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 RD

NOT USED
 LAST REF
 C8
 D11
 H3
 R44
 SM4
 U12



80-5027-A
Sub

All Components With Out Outlines
Are Installed On Solder Side



FUNCTIONAL PIN DESCRIPTION FOR HISC

<u>Description</u>	<u>Pin</u>
VSS: ground (GND)	1,20,32,43,54
CLK: oscillator input	2
TEST: in-house test only (GND)	3
GATE: in-house test only (GND)	4
OVRFLO: indicates internal math overflow	5
SHL: sample/hold left	6
SHR: sample/hold right	7
D: DAC compare input	8
LSREG: clocks lower byte DAC output	9
MSREG: clocks upper byte DAC output	10
VDD: +5V power	11,42,74
DAC7..DAC0: DAC output data	12,13,14,15,16,17,18,19
RAMADR7..RAMADR0: DRAM address output	21,22,23,24,25,26,27,28
RAS: DRAM row address strobe	29
DWR: DRAM write	30
CAS: DRAM column address strobe	31
DATA19..DATA0: DRAM data	33,34,35,36,37,38,39,40,41,44,45,46,47,48,49,50,51,52,53,55
MCODE0..MCODE15: microcode data	56,57,58,59,60,61,62,63,64,65,66,67,68,69,70,71
MCA0..MCA7: microcode address	72,73,75,76,77,78,79,80
ENEX: enable external microcode write	81
SWR: external microcode write line	82
RQUD: request for microcode update	83
I2K: in-house test only (+5V)	84